What is claimed is:

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42. (Original) A method of making a fuel cell, the method comprising the steps of:

creating a well in a dielectric or semiconductor substrate, the substrate having a first side and a second side, the second side opposed to the first side, and the well being defined in the first side;

depositing a thin film solid oxide electrolyte layer on the surface of the well;

applying an electrode layer in the electrolyte coated well;

creating a counter well in the second side, the counter well abutting the electrolyte layer; and

applying a counter electrode layer in the counter well.

43. (Original) The method as defined in claim 42 wherein the step of depositing the electrolyte layer is performed by at least one of sputter deposition and chemical vapor deposition (CVD).

44. (Original) The method as defined in claim 42, further comprising the step of firing the electrolyte layer prior to application of the electrode layer.

45. (Original) The method as defined in claim 42, further comprising the step of applying an isolation dielectric on the second side of the substrate.

46. (Original) The method as defined in claim 42 wherein the substrate is silicon, and wherein the isolation dielectric is grown on the second side of the substrate.

47. (Original) The method as defined in claim 42, further comprising the step of processing the electrode layer and the counter electrode layer using planarization techniques.

48. (Original) The method as defined in claim 42 wherein the planarization is performed by at least one of chemical mechanical polishing (CMP) and mechanical polishing.

49. (Original) The method as defined in claim 42, further comprising the step of applying a hard mask to the first side of the substrate before the step of creating a well.

50. (Original) The method as defined in claim 49 wherein the substrate is silicon, and wherein the first side hard mask is grown on the substrate first side.

51. (Original) The method as defined in claim 42, further comprising the step of applying a hard mask to the second side of the substrate before the step of creating a counter well.

52. (Original) The method as defined in claim 51 wherein the substrate is silicon, and wherein the second side hard mask is grown on the substrate second side.

53. (Original) The method as defined in claim 42 wherein the step of creating the well and the step of creating the counter well are each carried out by etching.

54. (Original) The method as defined in claim 42 wherein the substrate is silicon, and wherein the etching is performed by an etchant selected from the group consisting of wet anisotropic etchants, plasma

anisotropic etchants, and mixtures thereof, thereby forming ultra-smooth surfaces on the well and the counter well.

55. (Original) The method as defined in claim 54 wherein the wet anisotropic etchants are selected from the group consisting of potassium hydroxide (KOH), tetramethyl ammonium hydroxide (TMAH), a mixture of potassium hydroxide and isopropyl alcohol, ammonium hydroxide, sodium hydroxide, cerium hydroxide, ethylene diamine pyrocatechol, and mixtures thereof.

56. (Original) The method as defined in claim 54 wherein the plasma anisotropic etchant is sulfur hexafluoride alternated with C_4F_8.

57. (Original) The method as defined in claim 42 wherein the substrate is a silicon oxide containing dielectric substrate, and wherein the etching is performed by a hydrofluoric containing isotropic etchant.

58. (Original) The method as defined in claim 42 wherein the substrate is selected from the group consisting of single crystalline silicon, polycrystalline silicon, silicon oxide containing dielectric substrates, alumina, sapphire, ceramic, and mixtures thereof.

59. (Original) The method as defined in claim 58 wherein the substrate is single crystalline silicon.

60. (Original) The method as defined in claim 42 wherein at least one of the well and the counter well is adapted to contain a thick film electrode layer.

61. (Original) The method as defined in claim 60 wherein the well contains a thick film electrode and the counter well contains a thick film counter electrode.

62. (Original) A method of making a fuel cell, the method comprising the steps of:

creating a well in a dielectric or semiconductor substrate, the substrate having a first side and a second side, the second side opposed to the first side, and the well being defined in the first side;

depositing a thin film solid oxide electrolyte layer on the surface of the well, wherein the step of depositing the electrolyte layer is performed by at least one of sputter deposition and chemical vapor deposition (CVD);

applying an electrode layer in the electrolyte coated well;

creating a counter well in the second side, the counter well abutting the electrolyte layer, wherein the step of creating the well and the step of creating the counter well are each carried out by etching;

applying an isolation dielectric on the second side of the substrate;

applying a counter electrode layer in the counter well; and

processing the electrode layer and the counter electrode layer using planarization techniques, wherein the planarization is performed by at least one of chemical mechanical polishing (CMP) and mechanical polishing.

63. (Original) The method as defined in claim 62, further comprising the step of firing the electrolyte layer prior to application of the electrode layer.

64. (Original) The method as defined in claim 62 wherein the substrate is silicon, and wherein the isolation dielectric is grown on the second side of the substrate.

65. (Original) The method as defined in claim 62, further comprising the step of applying a hard mask to the first side of the substrate before the step of creating a well.

66. (Original) The method as defined in claim 65 wherein the substrate is silicon, and wherein the first side hard mask is grown on the substrate first side.

67. (Original) The method as defined in claim 62, further comprising the step of applying a hard mask to the second side of the substrate before the step of creating a counter well.

68. (Original) The method as defined in claim 67 wherein the substrate is silicon, and wherein the second side hard mask is grown on the substrate second side.

69. (Original) The method as defined in claim 62 wherein the substrate is silicon, and wherein the etching is performed by an etchant selected from the group consisting of wet anisotropic etchants, plasma anisotropic etchants, and mixtures thereof, thereby forming ultra-smooth surfaces on the well and the counter well.

70. (Original) The method as defined in claim 69 wherein the wet anisotropic etchants are selected from the group consisting of potassium hydroxide (KOH), tetramethyl ammonium hydroxide (TMAH), a mixture of potassium hydroxide and isopropyl alcohol, ammonium hydroxide, sodium hydroxide, cerium hydroxide, ethylene diamine pyrocatechol, and mixtures thereof.

71. (Original) The method as defined in claim 69 wherein the plasma anisotropic etchant is sulfur hexafluoride alternated with C_4F_8.

72. (Original) The method as defined in claim 62 wherein the substrate is a silicon oxide containing dielectric substrate, and wherein the etching is performed by a hydrofluoric containing isotropic etchant.

73. (Original) The method as defined in claim 62 wherein the substrate is selected from the group consisting of single crystalline silicon, polycrystalline silicon, silicon oxide containing dielectric substrates, alumina, sapphire, ceramic, and mixtures thereof.

74. (Original) The method as defined in claim 73 wherein the substrate is single crystalline silicon.

75. (Original) The method as defined in claim 62 wherein at least one of the well and the counter well is adapted to contain a thick film electrode layer.

76. (Original) The method as defined in claim 75 wherein the well contains a thick film electrode and the counter well contains a thick film counter electrode.

77. (New) A method of making a fuel cell, the method comprising the steps of:

depositing an electrolyte layer having a first surface and a second surface within a recess within a dielectric or semiconductor substrate, the first surface being opposed to the second surface;

depositing one of an anode layer and a cathode layer on the electrolyte layer first surface; and

depositing the other of the cathode layer and the anode layer on the electrolyte layer second surface.

78. (New) The method as defined in claim 77 wherein the electrolyte layer is a thin film and wherein at least one of the anode layer or the cathode layer is a thick film.

79. (New) The method as defined in claim 77 wherein the substrate has opposed outer surfaces, and wherein at least one of the anode layer or

the cathode layer is substantially flush with one of the substrate opposed outer surfaces.

80. (New) The method as defined in claim 77, further comprising the step of etching the recess into the substrate prior to depositing the electrolyte layer.